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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,133	01/23/2004	Giovanni Cesura	851863.410	6100

38106 7590 01/11/2005

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EXAMINER	
MAI, LAM T	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,133	CESURA ET AL.	
	Examiner	Art Unit	
	LAM T. MAI	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10* is/are allowed.

6)☒ Claim(s) *1,9,11 and 13* is/are rejected.

7)☒ Claim(s) *2-8,12,14-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,9, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Allworth et al. (USP 6486820).

Regarding claim 1, Allworth discloses in figure 4 a pipeline analog to digital converter that teaches a pipeline architecture (400) for converting an analog input signal (403) into a digital output signal with a predefined resolution, wherein the converter includes a plurality of stages (409,405)) each one having means (503) for converting an analog local signal into a digital local signal with a local resolution lower than said resolution, means (505) for determining an analog residue indicative of a quantization error of the means for converting, and means (507) for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and wherein the converter further includes means (415) for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, characterized in that the means for combining includes, for at least one of the stages, means for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means (417) for controlling the digital weight according to the digital correction signal (see col. 5,6,7).

Regarding claim 9, Allworth teaches at least one stage consists of a sub-set of consecutive stages starting from a first stage (see figures 4 and 5).

Regarding claim 11, Allworth discloses in figure 4 a pipeline analog to digital converter that teaches a pipeline architecture (400) for converting an analog input signal (403) into a digital output signal with a predefined resolution, wherein the converter includes a plurality of stages (409,405)) each one having means (503) for converting an analog local signal into a digital local signal with a local resolution lower than said resolution, means (505) for determining an analog residue indicative of a quantization error of the means for converting, and means (507) for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and wherein the converter further includes means (415) for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, characterized in that the means for combining includes, for at least one of the stages, means for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means (417) for controlling the digital weight according to the digital correction signal (see col. 5,6,7).

Regarding claim 13, Allworth discloses in figure 4 a pipeline analog to digital converter that teaches a pipeline architecture (400) for converting an analog input signal (403) into a digital output signal with a predefined resolution, wherein the converter includes a plurality of stages (409,405)) each one having means (503) for converting an analog local signal into a digital local signal with a local resolution lower than said resolution, means (505) for determining an analog residue indicative of a quantization

error of the means for converting, and means (507) for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and wherein the converter further includes means (415) for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain, characterized in that the means for combining includes, for at least one of the stages, means for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means (417) for controlling the digital weight according to the digital correction signal (see col. 5,6,7).

Allowable Subject Matter

Claims 2-8 are objected to as being dependent upon a rejected base claim, but they would be considered for allowable if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art fails to teach or suggest the means for estimating includes means for inputting a digital test signal into the at least one stage and means for deriving the digital correction signal from the digital test signal and the digital local signals of the next stages.

claim 10 is allowable, The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to teach or suggest a method for converting analog input into a digital output with a predetermined resolution.

Claim 12 is objected to as being dependent upon a rejected base claim, but it would be considered for allowable if it is rewritten in independent form including all of

the limitations of the base claim and any intervening claims. The prior art fails to teach or suggest an estimation circuit for inputting an digital test signal.

Claims 14-15 are objected to as being dependent upon a rejected base claim, but they would be considered for allowable if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art fails to teach or suggest a combining circuit including a digital test signal generator for inserting a test signal into at least the first stage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAM T. MAI whose telephone number is (571)272-1807. The examiner can normally be reached on 6:00 am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lam T. Mai
Art Unit 2819